Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): Circuit configuration, in particular for identifying error situations in interconnected partial systems ~~(20a, 20b, 20c)~~ for voltage generation in a fuel cell system, with

- an electrical signal line loop [[(10)]],

- several partial systems ~~(20a, 20b, 20c)~~ connected thereto, which evaluate the state of the signal line loop [[(10)]], wherein a first selectable switching means [[(40)]] is looped in between a first end [[(11)]] of the signal line loop [[(10)]] and a first voltage connection [[(30)]] and a second selectable switching means [[(41)]] is looped in between a second end [[(12)]] of the signal line loop [[(10)]] and a second voltage connection; and

- a selection unit [[(60)]] for selecting the first [[(40)]] and the second switching means [[(41)]].

Claim 2 (currently amended): Circuit configuration to claim 1, characterised in that a first impedance [[(50)]] is switched parallel to the first switching means [[(40)]] and a second impedance [[(51)]]is switched parallel to the second switching means [[(41)]].

Claim 3 (currently amended): Circuit configuration according to claim 1 [[or 2]], characterised in that the first voltage connection [[(30)]] is a supply voltage connection for the partial systems ~~(20a, 20b, 20c)~~.

Claim 4 (currently amended): Circuit configuration according to ~~one of claims 1 to 3~~ claim 1, characterised in that the second voltage connection [[(31)]] is a ground connection.

Claim 5 (currently amended): Circuit configuration according to ~~one of the preceding claims~~ claim 1, characterised in that the first switching means [[(40)]] is a transistor.

Claim 6 (currently amended): Circuit configuration according to ~~one of the preceding claims~~ claim 1, characterised in that the second switching means [[(41)]] is a transistor.

Claim 7 (currently amended): Circuit configuration according to ~~claims 5 and 6~~ claim 5, characterised in that the first [[(40)]] and the second transistor [[(41)]] are transistors complementary to one another.

Claim 8 (currently amended): Circuit configuration according to ~~one of claims 2 to 7~~ claim 2, characterised in that the first [[(50)]] and the second impedance [[(51)]] are ohmic resistors.

Claim 9 (currently amended): Circuit configuration according to ~~one of the preceding claims~~ claim 1, characterised in that the partial systems ~~(20a, 20b, 20c)~~ are connected to the signal line loop [[(10)]] with high resistivity.

Claim 10 (currently amended): Circuit configuration according to ~~one of the preceding claims~~ claim 1, characterised in that the signal line loop [[(10)]] is looped through the partial systems ~~(20a, 20b, 20c)~~.

Claim 11 (currently amended): Circuit configuration according to ~~one of the preceding claims~~ claim 1, characterised in that the partial systems ~~(20a, 20b, 20c)~~ have means [[(21)]] for interrupting the signal line loop [[(10)]] depending on their functional stage.

Claim 12 (currently amended): Method for identifying error situations of an electrical signal line loop [[(10)]] with several partial systems ~~(20a, 20b, 20c)~~ connected thereto, in particular partial systems ~~(20a, 20b, 20c)~~ for voltage generation in a fuel cell system, characterised by the steps:

- charging a first end [[(11)]] of the signal line loop [[(10)]] with a first voltage of a first voltage connection [[(30)]] and connecting a second end [[(12)]] of the signal line loop [[(10)]] to a second voltage connection [[(31)]] via second impedance [[(51)]],

- alternating with this, connecting the first end [[(11)]] to the first voltage connection [[(30)]] via a first impedance [[(50)]] and charging the second end [[(12)]] with the second voltage of the second voltage connection [[(31)]]; and

- measuring and evaluating the signal course on the signal line loop [[(10)]] to identify the error situation.

Claim 13 (currently amended): Method according to claim 12, characterised in that, during evaluation of the signal course is detected which partial systems ~~(20a, 20b, 20c)~~ constantly measure the first voltage, which partial systems ~~(20a, 20b, 20c)~~ measure an undefined voltage and which partial systems ~~(20a, 20b, 20c)~~ constantly measure the second voltage and in that short-circuits or short-circuits to ground and/or interruptions of the signal line loop [[(10)]] are ascertained and/or located as a function of the voltages measured by the individual partial systems ~~(20a, 20b, 20c)~~.

Claim 14 (currently amended): Method according to claim 12 [[or 13]], characterised in that, during evaluation of the signal course, an error is identified if at least one partial system ~~(20a, 20b, 20c)~~ measures a DC voltage.

Claim 15 (currently amended): Method according to ~~one of claims 12 to 14~~ claim 12, characterized in that, during evaluation of the signal course, a short-circuit of the signal line loop [[(10)]] with the first voltage connection [[(30)]] is identified if all the partial systems ~~(20a, 20b, 20c)~~ measure a DC voltage with the level of the first voltage connection [[(30)]].

Claim 16 (currently amended): Method according to ~~one of claims 12 to 15~~ claim 12, characterised in that, during evaluation of the signal course, a short-circuit of the signal line loop [[(10)]] with the second voltage connection

[[(31)]] is identified if all the partial systems ~~(20a, 20b, 20c)~~ measure a DC voltage with the level of the second voltage connection [[(31)]].

Claim 17 (currently amended): Method according to ~~one of claims 12 to 16~~ claim 12, characterised in that, during evaluation of the signal course, an interruption at a location on the signal line loop [[(10)]] is identified if partial systems ~~(20a, 20b, 20c)~~ on one side of the location constantly measure the first voltage and partial systems ~~(20a, 20b, 20c)~~ on the other side of the location constantly measure the second voltage.